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Date: December 22, 2003

To: **Examiner Eric W. Thomas**
Art Unit: 2831

Fax No.: 703/746-4138

From: Gina Husak for Stephen P. Burr

Subject: U.S. Application Ser. No. **10/057,804**
Filed: January 25, 2002
Conf. No.: 9257
Title: ELECTROSTATIC CHUCK AND SUBSTRATE PROCESSING APPARATUS

Our Ref.: 782_215

You should receive 20 page(s) **including this cover sheet.** If you do not receive all pages, please call (315) 233-8300.

Examiner Thomas,

Per our phone conversation today, attached is the Verified English-language translation of priority document JP '487 for the above-identified application, and our postcard receipt showing receipt by PTO on November 21, 2003.

Thank you!

Gina

IMPORTANT - THIS MESSAGE IS INTENDED ONLY FOR THE USE OF THE INDIVIDUAL OR ENTITY TO WHICH IT IS ADDRESSED, AND MAY CONTAIN INFORMATION THAT IS PRIVILEGED, CONFIDENTIAL AND EXEMPT FROM DISCLOSURE UNDER APPLICABLE LAW. IF THE READER OF THIS MESSAGE IS NOT THE INTENDED RECIPIENT, OR THE EMPLOYEE OR AGENT RESPONSIBLE TO DELIVER IT TO THE INTENDED RECIPIENT, YOU ARE HEREBY NOTIFIED THAT READING, DISSEMINATING, DISTRIBUTING OR COPYING THIS COMMUNICATION IS STRICTLY PROHIBITED. IF YOU HAVE RECEIVED THIS COMMUNICATION IN ERROR, PLEASE IMMEDIATELY NOTIFY US BY TELEPHONE, AND DESTROY THE COMMUNICATION. THANK YOU.

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Amendment Transmittal with Petition for Extension of Time (2 mos.) in duplicate	2 sheets
Amendment (pp.1-13)	13 sheets
Appendix A - Verified English-language translation of priority document JP '487	18 sheets
Information Disclosure Statement	1 sheet
form PTO1449	1 sheet
IDS transmittal (in duplicate)	2 sheets
1 reference (AA)	10 sheets
and our check in the amount of $600.00	

CIPE JC13 NOV 21 2003 PATENT & TRADEMARK OFFICE

for: (782_215 - mailing date: November 21, 2003) SPB/NB/gmh
Hideyoshi TSURUTA, Satoru YAMADA, Kiyoshi NASHIMOTO and Naoki MIYAZAKI
Serial No.: 10/057,804
Filed: January 25, 2002
Art Unit: 2831
For: ELECTROSTATIC CHUCK AND SUBSTRATE PROCESSING APPARATUS

COPY

SWORN TRANSLATION

I, Jun INOH, hereby declare and state that I am knowledgeable of each of the English and Japanese languages and that I made the attached translation of the certified copy of Japanese Patent Application No. 2001-019487 from the Japanese language into English language and that I believe my attached translation to be accurate, true and correct to the best of my knowledge and ability.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: November 10, 2003

Declarant: Jun Inoh

Jun INOH

Appendix A
filed 11-21-03

2001-019487

[Identification of Document]	Petition for Patent Application
[Reference Number]	01P00046
[Date of Submission]	January 29, 2001
[Addressee]	Commissioner, Patent Office: Kozo OIKAWA
[International Patent Classification]	C30B 25/00
[Title of Invention]	ELECTROSTATIC CHUCK AND SUBSTRATE PROCESSING APPARATUS
[Number of Claims]	4
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2001-019487

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[Deposit Account Number] 074997
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[Identification of Document] Specification

[Title of the Invention] ELECTROSTATIC CHUCK AND SUBSTRATE PROCESSING APPARATUS

[Claims]

[Claim 1] An electrostatic chuck having an insulation layer including a mount plane on which a wafer is mounted, an inner electrode provide in the insulation layer, and projecting portions protruded from the mount plane which include contact planes to be contacted to the wafer, wherein a backside gas is flowed in a space defined by the mount plane, the projecting portions, and the wafer under such a condition that the wafer is attracted to the mount plane so as to maintain a temperature uniformity of the wafer, comprising a construction such that a total amount of areas of the contact planes of the projecting portions is not less than 5% and not more than 10% with respect to an area of the inner electrode, and heights of the projecting portions are not less than 5 μm and not more than 10 μm.

[Claim 2] The electrostatic chuck according to claim 1, wherein diameters of the projecting portions are not less than 1.0 mm and not more than 2.0 mm.

[Claim 3] The electrostatic chuck according to claim 1 or 2, wherein the projecting portions are aligned side-by-side continuously.

[Claim 4] A substrate processing apparatus wherein a predetermined process is applied to a plane of a substrate, comprising: a process chamber in which the predetermined process is performed; the electrostatic chuck set forth in any one of claims 1 to 3, used for electrostatically attracting and holding the substrate at a predetermined position in the process chamber; and a power source for attracting used for electrostatically attracting the substrate to the electrostatic chuck.

[Detailed Description of Invention]

[0001]

[Technical Field of the Invention] The present invention relates to an electrostatic chuck which can achieve a uniform temperature distribution of a wafer and suppress a particle generation.

[0002]

[Prior Art] At present, electrostatic chucks are used for attracting and holding semiconductor wafers in finely working e.g., transferring, exposing, film-forming by CVD, washing, etching, and dicing the semiconductor wafers. Normally, a

plurality of projecting portions or embossed portions protruded from a mount plane of an insulation layer, and crown planes (contact planes) of the projecting portions are contacted to the semiconductor wafer. Moreover, DC voltage is applied to an inner electrode in the insulation layer, and Johnson-Rahbeck force is generated at a contact boundary between the semiconductor wafer and the projecting portions, so that the semiconductor wafer is attracted on the contact planes. Therefore, if an area of contact planes (crown planes) is increased, it is possible to improve an attraction of the semiconductor wafer.

[0003] Further, in order to perform predetermined processes such as film-forming and so on with respect to the semiconductor wafer, it is necessary to maintain a temperature of the semiconductor wafer at a constant temperature and to make a temperature at respective portions of the semiconductor wafer uniform. In this case, if a temperature of the insulation layer of the electrostatic chuck is increased by a built-in heater and so on, a heat is conducted from the insulation layer to the semiconductor wafer at a contact region between the contact planes of the projecting portions and a rear plane of the semiconductor wafer. However, in the method mentioned above, since a contacting state between the projecting portions and the semiconductor wafer is varied in accordance with a slight hardness variation of the contact planes of the projecting portions or a concavo-convex variation of a plane surface, a heat contacting resistance is varied at respective contact planes of respective projecting portions. Therefore, a heat from the insulation layer cannot be conducted stably to the overall semiconductor wafer, and thus a temperature uniformity of the semiconductor wafer is liable to be decreased. In order to eliminate such a drawback, there is proposed a method wherein a backside gas with a constant pressure is flowed through a space between the rear plane of the semiconductor wafer and the insulation layer, and a heat from the insulation layer is conducted to the semiconductor wafer by utilizing a heat radiation and a heat convection from the backside gas. In this case, if a pressure of the backside gas becomes larger, such tendencies are detected that, a heat conduction from the insulation layer to the semiconductor wafer becomes larger, and a temperature uniformity of the semiconductor wafer can be improved.

[0004]

[Problems to be Solved by the Invention] However, if an area of the contact planes of the projecting portions is made larger so as to improve an attraction of the semiconductor wafer, the rear plane of the semiconductor wafer and the contact planes of the projecting portions are robbed, so that particles are liable to generate. Such particles are deposited on the contact planes of the projecting portions and further there is a possibility such that they are adhered to the semiconductor wafer.

[0005] On the other hand, if an area of the contact planes of the projecting portions is made smaller, a particle generation is decreased and thus an adhesion of particles to the projecting portions is decreased. However, in this case, since Johnson-Rahbeck force acting between the contact planes and the semiconductor wafer is decreased, an attraction force of the semiconductor wafer is also decreased.

[0006] Further, when the backside gas with a predetermined pressure is flowed between the rear plane of the semiconductor wafer and the insulation layer, an ascending force due to the backside gas is applied to the semiconductor wafer. Therefore, an attraction force actually acting to the semiconductor wafer becomes such a value that an ascending force acting from the backside gas to the semiconductor wafer is taken from an attraction force due to electrostatic effects acting from the electrostatic chuck to the semiconductor wafer. In this case, if an area of the contact planes of the projecting portions is decreased as mentioned above, an ascending force acting to the semiconductor wafer becomes relatively larger, and thus an attraction force of the semiconductor wafer is not sufficient. In order to eliminate such a drawback, if a pressure of the backside gas is made smaller, a heat conduction due to the backside gas becomes insufficient, and thus a temperature uniformity of the semiconductor wafer is deteriorated.

[0007] An object of the present invention is to provide an electrostatic chuck having projecting portions protruded from a wafer mount plane, wherein a backside gas is flowed in a space defined by the wafer mount plane, the projecting portions and the wafer under such a condition that the wafer is attracted to the wafer mount plane so as to maintain a temperature uniformity of the wafer, which can reduce particles generated by robbing the projection portions and the wafer and improve a temperature uniformity of the wafer.

[0008]

[Means for Solving the Problems] According to the invention, an electrostatic chuck having an insulation layer including a mount plane on which a wafer is mounted, an inner electrode provide in the insulation layer, and projecting portions protruded from the mount plane which include contact planes to be contacted to the wafer, wherein a backside gas is flowed in a space defined by the mount plane, the projecting portions, and the wafer under such a condition that the wafer is attracted to the mount plane so as to maintain a temperature uniformity of the wafer, comprises a construction such that a total amount of areas of the contact planes of the projecting portions is not less than 5% and not more than 10% with respect to an area of the inner electrode, and heights of the projecting portions are not less than 5 μm and not more than 10 μm.

[0009] Moreover, according to the invention, a substrate processing apparatus wherein a predetermined process is applied to a plane of a substrate, comprises: a process chamber in which the predetermined process is performed; the electrostatic chuck used for electrostatically attracting and holding the substrate at a predetermined position in the process chamber; and a power source for attracting used for electrostatically attracting the substrate to the electrostatic chuck.

[0010] The present inventors found that, even in the case such that a total amount of areas of the contact planes of the projecting portions to be contacted to the wafer is made smaller to a level of not more than 10% with respect to an area of the inner electrode so as to reduce particle generations, if heights of the projecting portions are controlled to not less than 5 μm and not more than 10 μm, it is possible to effectively perform a heat conduction through the backside gas from the electrostatic chuck to the semiconductor wafer, and thus it is possible to maintain a high temperature uniformity of the semiconductor wafer.

[0011] This is further explained. Generally, a height of the projecting portion of the electrostatic chuck was about 20 μm, and a heat was conducted by a heat convection between the insulation layer and the semiconductor wafer. Therefore, it was thought that a low height of the projecting portion is not effective upon a heat conduction.

[0012] However, it was understood that, if a height of the projecting portion

is controlled actually to 5 - 10 μm, it is effective upon a heat conduction from another point of view. That is, it was assumed that coulomb force is acted between electric charges suspended near a plane of the insulation layer and electrostatic charges of the semiconductor wafer, other than an attraction force due to Johnson-Rahbeck force at a contact region between the projecting portions and the semiconductor wafer. Therefore, it was understood that an electrostatic attraction force of the semiconductor wafer is not decreased as expected. As a result, a pressure of the backside gas between the rear plane of the semiconductor wafer and the mount plane is made larger, and a heat conduction through the backside gas is effectively performed, so that it is possible to achieve a uniform temperature distribution of the semiconductor wafer. In order to obtain such advantages, it is necessary to set a height of the projecting portion to not more than 10 μm. From this point of view, it is more preferred to set a height of projecting portion to not more than 8 μm.

[0013] Moreover, it was understood that, if a height of the projecting portion is made smaller, a contribution of coulomb force mentioned above becomes larger, and an electrostatic attraction force is further improved. However, in the case such that a height of the projecting portion becomes less than 5 μm, a heat conduction efficiency was decreased even if a pressure of the backside gas was made larger, and thus a temperature uniformity of the semiconductor wafer was decreased. Assumably, it was understood that, if a height of the projecting portion becomes less than 5 μm, a heat convection is not contributed and thus a heat conduction is mainly performed by a heat radiation. Moreover, it is understood that, since the particles on the mount plane 2a are not directly contacted to the semiconductor wafer but are attracted electrostatically to the semiconductor wafer, it is difficult to reduce the particles from the semiconductor wafer. From this point of view, it is further preferred to set a height of the projecting portion to not less than 6 μm.

[0014] Further, if a total amount of areas of the contact planes of the projecting portions to be contacted to the wafer is less than 5% with respect to an area of the inner electrode, an attraction force is lowered excessively even with taking into consideration of a contribution of coulomb force mentioned above, and thus it is not possible to flow the backside gas with a sufficiently high

pressure, so that a temperature uniformity of the semiconductor wafer is decreased.

[0015] From the above point of view, it is further preferred to set a total amount of areas of the contact planes of the projecting portions to be contacted to the wafer to not more than 8% and not less than 6% with respect to an area of the inner electrode.

[0016] An area of the contact plane of the projecting portion to be contacted to the wafer means an area contacting to the rear plane of the wafer during a normal wafer attracting state. This is normally equal to an area of a top plane of the projecting portion. In this case, if some projecting portions have a low height and they are not contacted to the rear plane of the wafer during a normal wafer mounting state, top planes of those projecting portions are not included in this area.

[0017] Moreover, both of an area of the inner electrode and an area of the contact plane of the projecting portion means the area measured from a vertical direction with respect to the mount plane.

[0018] A height of the projecting portion is measured by a dial-gauge or a three-dimensional shape measuring apparatus.

[0019] Kinds of the processes with respect to the substrate are not limited, but mention may be made of finely working e.g., transferring, exposing, film-forming by CVD, washing, etching, and dicing the semiconductor wafers.

[0020] A kind of the substrate is not limited, but it is preferred to use the semiconductor wafer.

[0021] As the chamber and the power source for electrostatically attracting, use may be made of the known members in their technical fields.

[0022] Fig. 1 is a plan view showing one embodiment of an electrostatic chuck 1 according to the invention. Fig. 2 is a partially enlarged cross sectional view illustrating the electrostatic chuck shown in Fig. 1.

[0023] In the embodiment shown in Fig. 1, the electrostatic chuck 1 comprises an insulation layer 2 having a disc shape and an inner electrode 12 embedded in the insulation layer 2. A numeral 2b is a side plane (outer surface) of the insulation layer 2, and a numeral 2a is a planar mount plane of the insulation layer 2. Plural projecting portions 3A are protruded from the mount

plane 2a. Respective projecting portions 3A has a plate shape more preferably a disc shape. The projecting portions 3A are separated with each other, and they are scattered on the mount plane 2a.

[0024] Moreover, gas supply holes 6 are formed in the insulation layer 2 at for example three positions in this embodiment, and a gas distribution recess 5 is communicated with upper end portions of the gas supply holes 6. The gas distribution recess 5 comprises depression portions 5a continuing from the gas supply holes 6, long recesses 5b extending toward the side plane 2b from the depression portion 5a, and a circular recess 5c continuing from a tip portion of respective recesses 5b. The gas distribution recess 5 is formed at a lower position with respect to the mount plane 2a. Therefore, as shown in Fig. 2, when a backside gas is supplied to the gas supply hole 6 as shown by an arrow A, the backside gas is introduced into the depression portion 5a as shown by an arrow B, which is flowed through the recesses 5b and 5c. In this case, the backside gas is flowed into a space 11 defined by the mount plane 2a, the projecting portions 3A and a semiconductor wafer 10 from all of the recesses 5b and 5c.

[0025] At a center portion of the insulation layer 2, a circular through hole 7 and recesses 8 extending radial toward peripheral three directions are formed. The projecting portions are not formed near the through hole 7 and the recess 8.

[0026] According to the invention, a total amount of areas of top planes 14 (contact planes to the semiconductor wafer) of the projection portions 3A is not less than 5% and not more than 10% with respect to an area of the inner electrode 12. Moreover, a height H of the projecting portion is set to not less than 5 μm and not more than 10 μm.

[0027] In the present invention, a diameter ϕ of respective projecting portions can be varied in various ways, but it is preferred to set such a diameter to 1.0 - 2.0 mm from a point of view of achieving a temperature uniformity of the wafer.

[0028] Moreover, a two-dimensional shape and a two-dimensional size are varied in various ways. For example, a shape of the contact plane of the projecting portion may be polygonal shape such as triangular shape, quadrangle shape, hexagonal shape, octagonal shape and so on other than circular shape. Moreover, the number of the projecting portions is not particularly limited.

However, in order to make an attraction force with respect to the semiconductor wafer uniform on all the planes of the semiconductor wafer, it is particularly preferred to set the number of the projecting portions per a unit area to 0.010 - 0.140 piece/mm^2.

[0029] It is preferred to align the projecting portions side-by-side continuously. In this case, it is possible to reduce a lack in uniformity of the attraction force of the wafer and to further improve a temperature uniformity of the wafer. Here, a term "align the projecting portions side-by-side continuously" means that, when viewed from a direction parallel to the attraction plane as shown in Fig. 3 for example, the projecting portions 3A and the recesses between the projecting portions 3A are arranged alternately. Preferably, the projecting portions 3A are arranged regularly with a predetermined constant interval.

[0030] Materials of the insulation layer are not limited, but it is preferred from a point of view of further reducing a particle generation to use ceramics of aluminum nitride series, composite materials including aluminum nitride, ceramics of alumina series, composite materials including alumina, and composite ceramics of alumina and aluminum nitride.

[0031] Materials of the inner electrode are not also limited, and use may be made of conductive ceramics and metals, but it is preferred to use a metal having a high melting point such as molybdenum, tungsten, and alloy of molybdenum and tungsten.

[0032] Materials of the projecting portions are not particularly limited, but it is preferred from a point of view of further reducing the particle generation to use ceramics of aluminum nitride series, composite materials including aluminum nitride, ceramics of alumina series, composite materials including alumina, and composite ceramics of alumina and aluminum nitride. The projecting portions are formed by blast working, chemical vapor epitaxy method and so on.

[0033] As the backside gas, use may be made of known gasses such as helium gas, argon gas, and a mixture gas of helium gas and argon gas.

[0034] In order to improve a heat conductivity to the semiconductor wafer, it is preferred to set a pressure for supplying the backside gas to the gas supply hole to not less than 5 Torr more preferably not less than 15 Torr. In this case, if this pressure is increased excessively, an attraction force to the wafer is decreased

and the wafer is liable to deviate. Therefore, it is preferred to set this pressure to not more than 30 Torr.

[0035]

[Examples] The electrostatic chuck having the shape shown in Figs. 1 and 2 was produced. Specifically, aluminum nitride powders were formed into a specific shape to obtain a formed body. Then, the inner electrode made of molybdenum was arranged on the thus obtained formed body, and aluminum nitride powders are filled thereon. After that, the forming process was performed again to obtain the disc-shaped formed body in which the inner electrode was embedded. Then, the thus obtained formed body was sintered in nitrogen atmosphere to produce the insulation layer 2 having a diameter of 200 mm in which the inner electrode was embedded.

[0036] Then, plural projection portions 3A each having a two-dimensionally circular shape as shown in Fig. 1 were formed on a front plane of the insulation layer 2 by a blast working. Moreover, the through hole 7 and the gas distribution recess 5 were formed.

[0037] An area of the inner electrode 12 was 31000 mm^2. By varying an area of the contact plane 14 of the projecting portion 3A and the number of the projecting portions 3A in various ways, percentages of total amounts of the areas of the contact planes 14 with respect to an area of the inner electrode 12 were varied as shown in the following Table 1 and Table 2. Moreover, the heights H of the projecting portions 3A were also varied as shown in the following Table 1 and Table 2.

[0038] The silicon wafer 10 having a diameter of 200 mm was mounted on the mount plane 2a of the electrostatic chuck 1. The rear plane of the silicon wafer 10 was contacted to the contact planes 14 of the projecting portions 3A. DC voltages of ±500 V were applied to the inner electrode 12 so as to attract the silicon wafer 10 to the electrostatic chuck 1. Then, an electrostatic attraction force of the silicon wafer was measured at a pressure (Torr) unit under such a condition that the backside gas was not flowed.

[0039] Then, argon gas was supplied into the space 11 defined by the silicon wafer 10, the insulation layer 2 and the projecting portions 3A as mentioned above. By heating the insulation layer 2, an average temperature of the silicon

wafer was increased to 350°C. The pressure for supplying the backside gas was controlled in such a manner that an attraction force of the silicon wafer after supplying the backside gas was maintained at about 30 Torr. Under such a condition, temperatures of the silicon wafer were measured at five points by using the wafer with thermocouple, and a temperature difference between the maximum and the minimum was obtained.

[0040] Moreover, after the silicon wafer was attracted for one minute at 350°C as mentioned above, the attraction of the silicon wafer was ceased. Then, the number of the particles adhered to the rear plane of the silicon wafer was counted by using the particle counter utilized normally in the semiconductor manufacturing factory. These results were shown in Table 1 and Table 2.

[0041]

[Table 1]

Percentage of areas of contact planes of projection portions with respect to area of inner electrode (%)	3	5	7	10	15
Height of projecting portion H (mm)	7	7	7	7	7
Electrostatic attraction (g/mm^2) (no backside gas)	40	more than 50	more than 50	more than 50	more than 50
Temperature difference of silicon wafer between maximum and minimum (°C)	±5	±3	±2	±3	±3
The number of particles (piece/mm^2)	2	2	3	5	20

[0042]

[Table 2]

Percentage of areas of contact planes of projection portions with respect to area of inner electrode (%)	7	7	7	7	7
Height of projecting portion H (mm)	3	5	7	10	15
Electrostatic attraction (g/mm^2) (no backside gas)	more than 50	more than 50	more than 50	more than 50	25
Temperature difference of silicon wafer between maximum and minimum (°C)	±10	±3	±2	±3	wafer peeling due to gas pressure
The number of particles (piece/mm^2)	20	5	3	5	–

[0043]

[Effect of the Invention] According to the electrostatic chuck of the present invention, it is possible to reduce the particles generated due to the robbing between the projecting portions and the semiconductor wafer, and also it is possible to improve of the temperature uniformity of the semiconductor wafer.

[Brief Description of the Drawings]

[Fig. 1] A plan view showing one embodiment of an electrostatic chuck 1 according to the invention.

[Fig. 2] A partially enlarged cross sectional view illustrating the electrostatic chuck shown in Fig. 1.

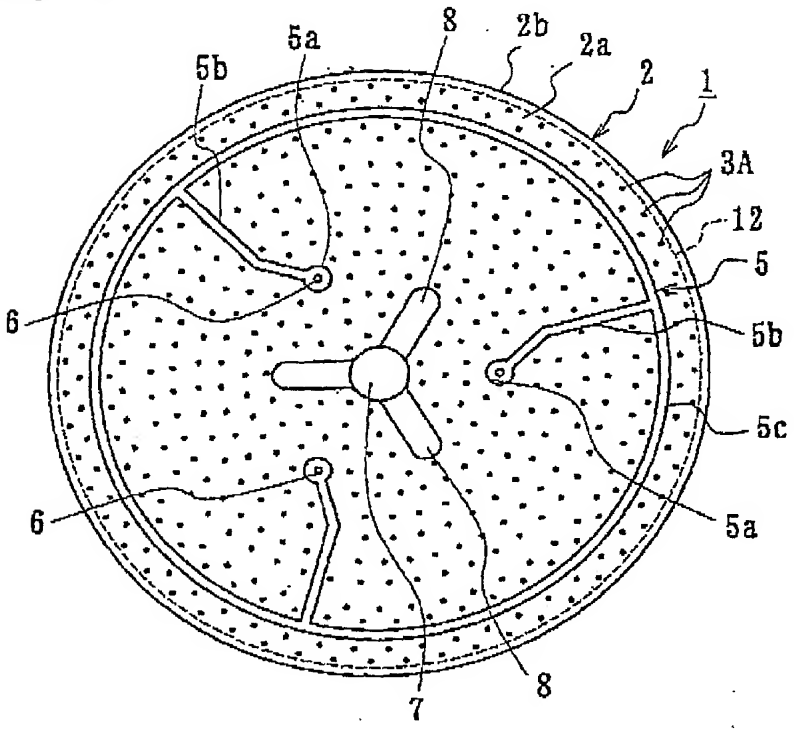
[Fig. 3] A schematic view depicting a state such that projecting portions are aligned side-by-side on a plane of the electrostatic chuck.

[Description of the Numerals]

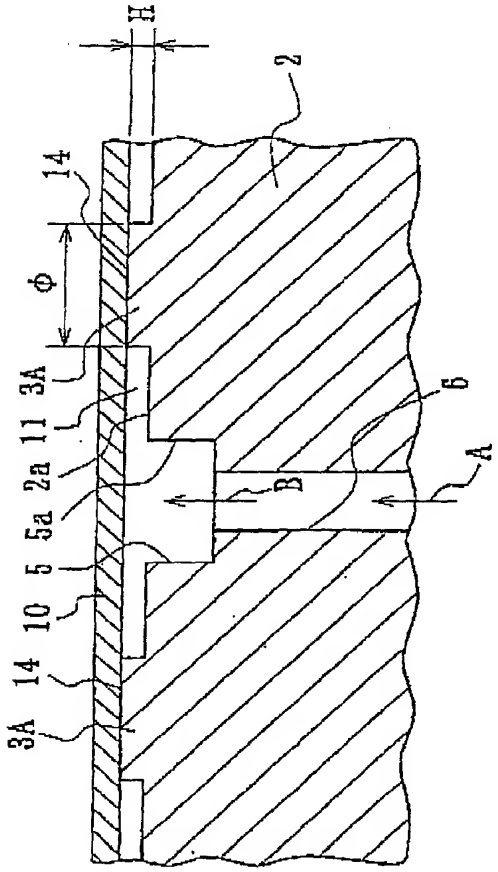
1 electrostatic chuck
2 insulation layer
2a planar mount plane of the insulation layer
3A projecting portion contacting to wafer
7 through hole
5 gas distribution recess
6 gas supply hole
10 wafer
11 a space defined by the mount plane 2a, the projecting portions 3A, 3B and a wafer 10
12 inner electrode
14 contact plane of the projecting portion

提出日 平成１３年 １月２９日
整理番号＝０１Ｐ０００４６ 頁: 1/ 3

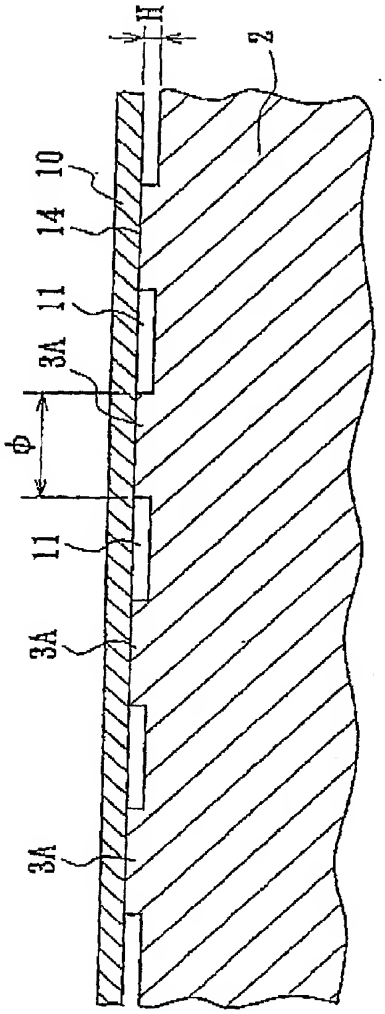
【書類名】 図面
[Identification of Document] Drawing
【図１】
[Fig. 1]



【図２】
[Fig. 2]



【図３】
[Fig. 3]



[Identification of Document] Abstract

[Abstract]

[Object]

In an electrostatic chuck, to reduce particles generated by robbing projection portions and a wafer and to improve a temperature uniformity of the wafer.

[Solving Means]

An electrostatic chuck 1 having an insulation layer 2 includes a mount plane 2a on which a wafer 10 is mounted, an inner electrode provide in the insulation layer 2, and projecting portions 3A protruded from the mount plane 2a which include contact planes 14 to be contacted to the wafer 10. A backside gas is flowed into a space 11 defined by the mount plane 2a, the projecting portions 3A, and the wafer 10 under such a condition that the wafer 10 is attracted to the mount plane so as to maintain a temperature uniformity of the wafer 10. A total amount of areas of the contact planes 14 of the projecting portions 3A contacting to the wafer 10 is not less than 5% and not more than 10% with respect to an area of the inner electrode, and heights H of the projecting portions 3A are not less than 5 μm and not more than 10 μm.

[Selected Figure] Fig. 2

PAGE 20/20 * RCVD AT 12/22/2003 1:36:29 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/2 * DNIS:7464138 * CSID:3152338320 * DURATION (mm-ss):04-54